JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY: KAKINADA
KAKINADA – 533 003, Andhra Pradesh, India

DEPARTMENT OF INFORMATION TECHNOLOGY

II Year – I Semester		L	T	P	C
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COMPUTER ORGANIZATION					

Course Objectives:
The course objectives of Computer Organization are to discuss and make student familiar with the

- Principles and the Implementation of Computer Arithmetic
- Operation of CPUs including RTL, ALU, Instruction Cycle and Busses
- Fundamentals of different Instruction Set Architectures and their relationship to the CPU Design
- Memory System and I/O Organization
- Principles of Operation of Multiprocessor Systems and Pipelining

Course Outcomes:
By the end of the course, the student will

- Develop a detailed understanding of computer systems
- Cite different number systems, binary addition and subtraction, standard, floating-point, and micro operations
- Develop a detailed understanding of architecture and functionality of central processing unit
- Exemplify in a better way the I/O and memory organization
- Illustrate the concepts of parallel processing, pipelining and inter processor communication

UNIT I
Basic Structure of Computers: Basic Organization of Computers, Historical Perspective, Bus Structures, Data Representation: Data types, Complements, Fixed Point Representation. Floating – Point Representation. Other Binary Codes, Error Detection Codes.
Computer Arithmetic: Addition and Subtraction, Multiplication Algorithms, Division Algorithms.

UNIT II
Register Transfer Language and Microoperations: Register Transfer language. Register Transfer Bus and Memory Transfers, Arithmetic Micro operations, Logic Micro Operations, Shift Micro Operations, Arithmetic Logic Shift Unit.
Basic Computer Organization and Design: Instruction Codes, Computer Register, Computer Instructions, Instruction Cycle, Memory – Reference Instructions. Input –Output and Interrupt, Complete Computer Description,

UNIT III
Central Processing Unit: General Register Organization, STACK Organization. Instruction Formats, Addressing Modes, Data Transfer and Manipulation, Program Control, Reduced Instruction Set Computer.
Microprogrammed Control: Control Memory, Address Sequencing, Micro Program example, Design of Control Unit

UNIT IV
Memory Organization: Memory Hierarchy, Main Memory, Auxiliary Memory, Associative Memory, Cache Memory, Virtual Memory.

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Input-Output Organization: Peripheral Devices, Input-Output Interface, Asynchronous data transfer, Modes of Transfer, Priority Interrupts, Direct Memory Access.

UNIT-V

Multi Processors: Introduction, Characteristics of Multiprocessors, Interconnection Structures, Inter Processor Arbitration.

Pipeline: Parallel Processing, Pipelining, Instruction Pipeline, RISC Pipeline, Array Processor.

Text Books:

1) Computer System Architecture, M. Morris Mano, Third Edition, Pearson, 2008.
2) Computer Organization, Carl Hamacher, Zvonko Vranesic, Safwat Zaky, 5/e, McGraw Hill, 2002.

Reference Books:

1) Computer Organization and Architecture, William Stallings, 6/e, Pearson, 2006.
2) Structured Computer Organization, Andrew S. Tanenbaum, 4/e, Pearson, 2005.
3) Fundamentals of Computer Organization and Design, Sivarama P. Dandamudi, Springer, 2006

e- Resources:

1) https://nptel.ac.in/courses/106/105/106105163/
2) http://www.cuc.ucc.ie/CS1101/David%20Tarnoff.pdf